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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,656	12/04/2001	Thomas A. Figura	303.645US2	1555

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EXAMINER
THOMAS, TONIAE M

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,656	FIGURA, THOMAS A.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,11-22 and 29-34* is/are allowed.

6)☒ Claim(s) *2-4, 6-10, 23-25, 27, 28, 35-40, 44, 47-52* is/are rejected.

7)☒ Claim(s) *5,26,41-43,45 and 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is an official response to the amendment filed on 13 May 2003. Currently, claims 1-52 are pending.

Allowability Withdrawn

2. The indicated allowability of claims 6 and 23-28 is withdrawn in view of the previously submitted references to Kim (US 5,569,948) and Juengling et al. (US 5,858,865). See information disclosure statement filed on 04 December 2001 as Paper No. 2. The indicated allowability of claim 10 is withdrawn in view of the previously cited reference to Jeng (US 6,080,620) and the newly cited reference to Ema (US 5.561,623). Rejections based on the references follow. The indicated allowability of claim 5 is withdrawn because claim 5, as amended, is a duplicate of claim 1. The objection to claim 5 follows.

Drawings

3. *The drawings are objected to under 37 CFR 1.83(a).* The drawings must show every feature of the invention specified in the claims. Therefore, the flash memory cells as recited in claims 1 and 5 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. *Claims 5 and 35-37 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 1-4.* When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. *Claims 2-4, 7-9, and 35-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.*

Since independent claims 1 and 5 recite the limitation "wherein the number of semiconductor surface structures includes flash memory cells," the integrated circuit device of claims 1 and 5 is clearly a flash EEPROM. However, the limitations of claims

2-4 and 7-9, which depend from claim 1, and the limitations of claims 35-40, which depend from claim 5, recite elements of DRAM memory cells. The limitations of dependent claims 2-4, 7-9, and 35-40 cannot recite elements of DRAM memory cells, since the integrated circuit of independent claims 1 and 5 is a flash EEPROM. Correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. *Claims 6, 23-25, 27, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim (US 5,569,948).*

Kim discloses an integrated circuit device on a substrate 1 (figs. 3, 4A-4F, and col. 4, line 31 - col. 5, line 59). The method comprises the following elements: a number of semiconductor surface structures spaced apart along the substrate (fig. 4C);[1] a number of plugs 12', 12" contacting the substrate between the number of surface structures (fig. 4D), wherein the number of plugs includes an inner plug 12' and a pair of outer plugs 12", each one of the outer pair being formed adjacent to and on opposing sides of the

[1] The spaced apart structures comprise gate insulating layer 3, gate electrode 4, insulating film 5, and patterned insulating film 10.

inner plug 12', [2] each one of the outer pair having upper portions, wherein the upper portions cover areas of the surface structures (fig. 4D and col. 5, lines 20-23); and an inner electrical contact 15 coupled to the inner plug and separated from the upper portions by a pair of opposing spacers 14 (fig. 4E), wherein the inner plug 12' is formed beneath a top surface of the number of semiconductor surface structures (fig. 4D).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. *Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Juengling et al (US 5,858,865).*

Kim does not teach that the number of plugs includes polysilicon plugs.

The Juengling et al. patent discloses a semiconductor device comprising contact plugs (e.g. fig. 10). The contact plugs are polysilicon plugs (col. 6, lines 49-56).

Since Kim and Juengling et al. both disclose an integrated circuit comprising conductive contact plugs, the polysilicon plugs disclosed by Juengling et al. would have

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[2] Only one outer plug 12" is shown in fig. 4D. However, it is inherent from figs. 3 that the blanket deposition and subsequent etching of conductive layer 12 results in a pair of outer plugs being formed (see figs. 3, 4C, 4D, and col. 4, line 66 - col. 5, line 20).

been recognized in the pertinent art of Kim by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one having ordinary skill in the art to modify the integrated circuit of Kim, at the time the invention was made, by using polysilicon contact plugs, as taught by Juengling et al., since polysilicon forms good adhesion with the silicon substrate, and does not require a separate adhesion layer or diffusion barrier layer as do metal layers, such as tungsten.

8. *Claims 10 and 47-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeng (6,080,620) in view of Ema (US 5,561,623).*

a. Jeng discloses an integrated circuit device on a substrate 10 (figs. 1-17 and accompanying text). The method comprises the following elements: a number of semiconductor surface structures 25 spaced apart along the substrate (fig. 2); a number of plugs 46, 48 contacting the substrate between the number of surface structures (fig. 11A), wherein the number of plugs includes an inner plug 48 and a pair of outer plugs 46, each one of the outer pair being formed adjacent to and on opposing sides of the inner plug 48, each one of the outer pair having upper portions, wherein the upper portions cover areas of the surface structures (fig. 11A); and an inner electrical contact 50 coupled to the inner plug and separated from the upper portions by a pair of opposing spacers 60 (figs. 11A, 12).

Each of two outer contacts 68 individually couples to one of the outer pair of plugs 46 (fig. 17). The outer plugs are storage node plugs 46, and the outer contacts 68 include storage nodes (col. 5, lines 1-2 and lines 25-27).

The surface structures 25, 27 are isolated word lines (col. 4, lines 11-16).

The plugs 46, 48, which are formed from layer 44, are polysilicon plugs (figs. 10, 11A, and col. 4, lines 54-58).

The inner plug 48 is a bit line plug, and the inner electrical contact 50 includes a bit line contact (col. 4, line 64 – col. 5, line 8).

The integrated circuit device includes a DRAM (col. 3, lines 21-23).

b. Jeng lacks anticipation only in not teaching that the DRAM is a synchronous random access memory.

c. Ema discloses a DRAM device (figs. 2A-2F and accompanying text). The DRAM device is a high-speed or synchronous DRAM (col. 1, lines 7-9). As its name implies high-speed DRAM devices are capable of transferring data at a high speed. The inputting/outputting of data is synchronized with a clock signal.

d. Since both Jeng and Ema disclose an integrated circuit comprising DRAM devices, the high-speed DRAM disclosed by Ema would have been recognized in the pertinent art of Jeng at the time of the invention by one of ordinary skill in the art.

e. One having ordinary skill in the art would have been motivated to modify Jeng, at the time the invention was made, to provide a synchronous DRAM because synchronous DRAM devices are capable of transferring data at a high speed.

Allowable Subject Matter

9. Claims 1, 11-22, and 29-34 are allowed. Claims 26, 41-43, 45, 46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 2-4 and 7-9 would be allowable if rewritten to overcome the rejection under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (703) 305-7646. The examiner can normally be reached on Monday through Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TMT
July 24, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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